Roll No. | | | | | | | | | | |

ANNA UNIVERSITY (UNIVERSITY DEPARTMENTS)
B.E. /B.Tech (Full Time) - END SEMESTER EXAMINATIONS, NOV / DEC.2024

ELECTRONICS AND COMMUNICATION ENGINEERING BRANCH
Semester III

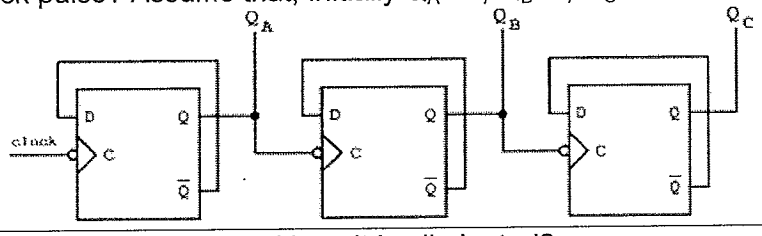
EC23C13 DIGITAL ELECTRONICS AND SYSTEM DESIGN
(Regulation2023)

Time:3 hrs | Max. Marks: 100

CO1	Ability to apply Boolean algebra and simplification procedure in digital logic systems.
CO2	Ability to design combinational digital circuits using logic gates.
CO3	Ability to analyze and design synchronous sequential circuits.
CO4	Ability to analyze and design asynchronous sequential circuits.
CO5	Ability to design digital circuits using MOS and PLDs.

BL – Bloom's Taxonomy Levels
(L1-Remembering, L2-Understanding, L3-Applying, L4-Analysing, L5-Evaluating, L6-Creating)

PART- A(10 x 2 = 20 Marks)
(Answer all Questions)

Q.No.	Questions	Marks	CO	BL
1	If $(54)_x = (49)_{10}$, then x is equal to _____	2	1	2
2	Simplify the expression xy + xy' + x'y using Boolean laws to minimum literals.	2	1	2
3	Write the necessary output expressions of 4-bit comparator.	2	2	2
4	Implement 8:1 Mux using 4:1 Mux and 2:1 Mux.	2	2	2
5	Construct a T flip flop from a D flip flop.	2	3	2
6	What is the output (Q_A,Q_B,Q_C) produced by the circuit in Fig.1 after 3rd clock pulse? Assume that, initially Q_A= 0, Q_B=1, Q_C=1.  Fig.1	2	3	2
7	Define essential hazard and how it is eliminated?	2	4	1
8	Outline the instability condition in asynchronous sequential circuits with an example.	2	4	1
9	What is Noise margin? How it is determined?	2	5	1
10	What is meant by CPLD and mention its important components.	2	5	1

PART- B(5 x 13 = 65 Marks)
(Restrict to a maximum of 2 subdivisions)

Q.No.	Questions	Marks	CO	BL
11 (a)	Simplify the given Boolean function using K-map and implement the resultant expression using universal gates. $f(w, x, y, z) = x'z' + y'z + w'xz + wyz'$ $d(w,x,y,z) = (x'+w)yz$	13	1	3
	OR			
11 (b)	For this function, find a minimum sum-of-products solution, using the Quine McCluskey method. $f(a, b, c, d) = \Sigma\, m(2,3,7,9,11,13) + \Sigma\, d(1, 10, 15)$.	13	1	3

12 (a) (i)	Realize a BCD to excess-3 code converter using a 4-to-10 decoder with active low outputs and a minimum number of gates.	9	2	3
(ii)	Design a full adder circuit using 4 to 1 multiplexers with logic gates.	4	2	3
	OR			
12 (b)	Discuss the working principle of 4-bit Ripple carry adder and 4-bit carry look-ahead adder with neat circuits and analyze the carry propagation time of both the circuits to show the circuit limits/improves the speed.	13	2	3
13 (a) (i)	A sequential circuit with two D flip flops A and B, two inputs x and y, and one output Z is specified by the following next state and output equations. $A(t+1) = x'y + xA$ $B(t+1) = xA + x'B$ and $Z = B$ Obtain the logic diagram, state table and state diagram.	7	3	4
(ii)	Reduce the state table shown in Fig.2 and verify the output sequences of original and reduced state tables with input sequence of 10110011. Draw the reduced state diagram.	6	3	4

Fig.2

Present state	Next state, Z (Output) X (Input) 0	1
A	A,0	B,0
B	C,0	D,0
C	A,0	D,0
D	E,0	F,1
E	A,0	F,1
F	G,0	F,1
G	A,0	F,1

	OR		
13 (b)	Develop a synchronous 3-bit up/down counter using J-K flip-flops. The counter should count up when a U/D control input is 1 and count down when the control input U/D is 0.	13	3	4
14 (a)	Draw the logic diagram for the expression F = AB' + BC. i) Identify the type of static hazard by analyzing the circuit with necessary input variation. ii) Write down the product-of-sums expression for the above expression. Do the same as given in (i). iii) Find the way(s) to remove the hazards.	13	4	4
	OR			
14 (b)	Find the critical race-free state assignment and design an asynchronous sequential circuit for the flow table shown in Fig.3 with and without SR NAND latches and gates.	13	4	4

Fig.3

State	Next State X_1X_2 = 00 01 10 11	Z
S_0	S_0 S_1 S_2 S_0	0
S_1	S_0 S_1 S_2 S_1	0
S_2	S_0 S_1 S_2 S_2	1

15 (a)	Draw a 4-input CMOS NAND circuit. Explain the operation denoting ON and OFF status of individual transistors under various input combinations. Repeat the same for a four-input CMOS NOR gate.	13	5	3
	OR			
15 (b)	Design a PLA circuit with PLA table for the following equations: X = AB'D + A'C' + BC + C'D' Y = (A'C' + AC + C'D')' Z = CD + A'C' + AB'D	13	5	3

PART- C(1x 15=15Marks)

(Q.No.16 is compulsory)

Q.No.	Questions	Marks	CO	BL
16. (i)	Implement the following four output expressions with three half adders: D = A ⊕ B ⊕ C E = A'BC + AB'C F = ABC' + (A' + B')C G = ABC	6	2	5
(ii)	Design an asynchronous sequential circuit that has two inputs X1 and X2 and one output Z. The output is to remain 0 as long as X1 is 0. The first change in X2 that occurs, while X1 is 1, will cause Z to be a 1. The output Z is to remain a 1 until X1 returns to 0. a) Construct a Primitive Flow Table b) Reduce the Primitive Flow Table using implication table and draw the reduced Flow table.	9	4	6